TS64MSS64V6F

144PIN PC133 Unbuffered SO-DIMM
512MB With 32Mx8 CL3

Description

Module (S.O.DIMM), mounted 16 pieces of 256-Mbit SDRAM sealed in TSOP package and 1 piece of serial EEPROM (2-kbit) for Presence Detect (PD). An outline of the products is 144-pin Zig Zag Dual tabs socket type compact and thin package. Therefore, they make high density mounting possible without surface mount technology. They provide common data inputs and outputs. Decoupling capacitors are mounted beside TSOP on the module board. Note: Do not push the cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.

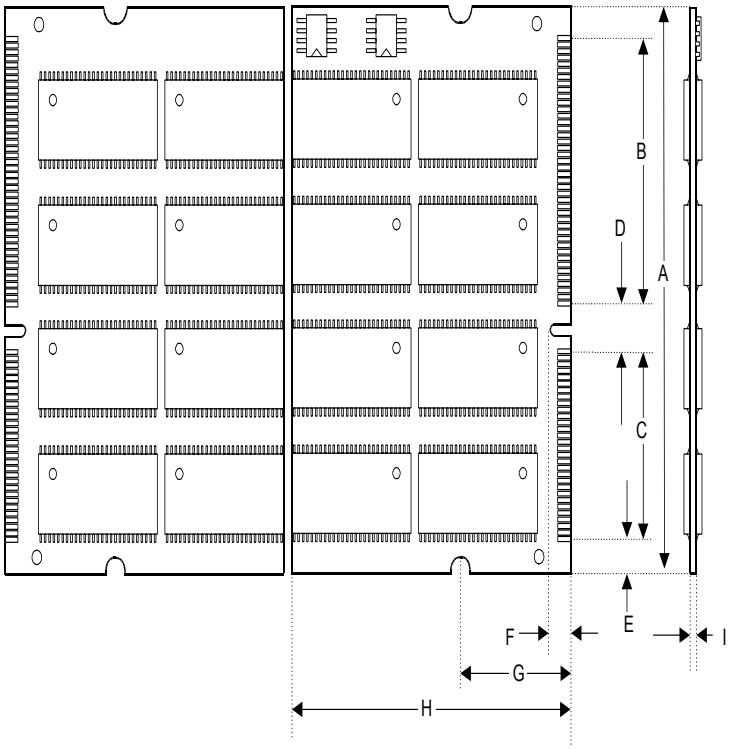
Features

- Performance Range : PC-133
- Conformed to JEDEC Standard Spec.
- Burst Mode Operation.
- Auto and Self Refresh.
- CKE Power Down Mode.
- DQM Byte Masking (Read/Write)
- Serial Presence Detect (SPD) with serial EEPROM
- LVTTL compatible inputs and outputs.
- Single 3.3V ± 0.3V power supply.
- MRS cycle with address key programs.
  Latency (Access from column address)
  Burst Length (1,2,4,8)
  Data Sequence (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.

Pin Identification

Symbol	Function
A0~A12,BA0,BA1	Address input
DQ0~DQ63,	Data Input / Output.
CLK0,CLK1	Clock Input.
CKE0,CKE1	Clock Enable Input.
/CS0~/CS3	Chip Select Input.
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
DQM0~DQM7	Data (DQ) Mask
SA0~SA2	Address in EEPROM
SCL	Serial PD Clock
SDA	Serial PD Add/Data input/output
Vcc	+3.3 Voltage Power Supply
Vss	Ground
NC	No Connection

Dimension :



PCB : 09-7265

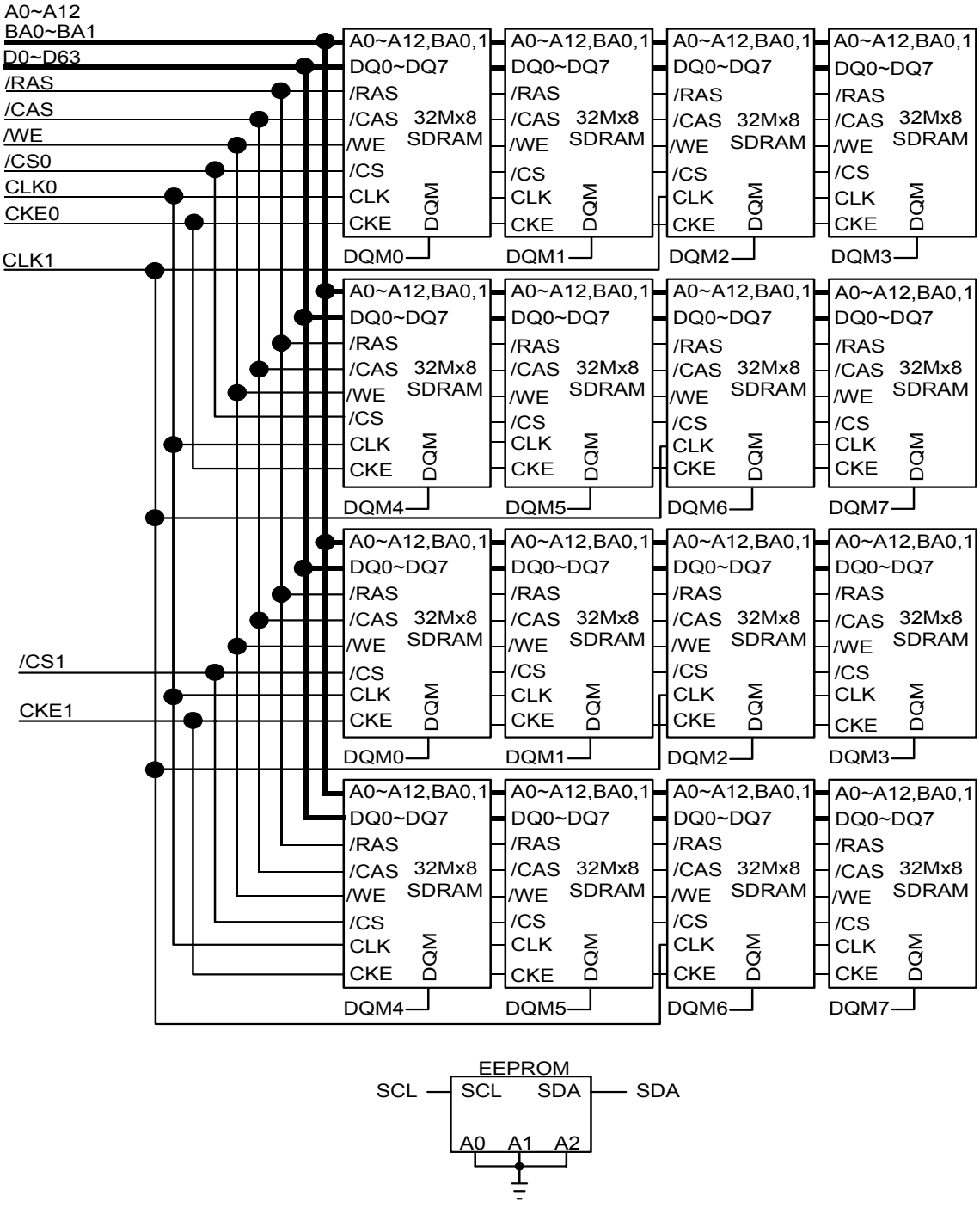
Side	Millimeters	Inches
A	67.60	2.661
B	32.80	1.291
C	23.20	0.913
D	4.60	0.181
E	3.30	0.130
F	4.00	0.157
G	20.00	0.787
H	50.50	1.988
I	1.00 ± 0.100	0.039 ± 0.004

Pinouts:

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	Vss	49	DQ13	97	DQ22	02	Vss	50	DQ45	98	DQ54
03	DQ0	51	DQ14	99	DQ23	04	DQ32	52	DQ46	100	DQ55
05	DQ1	53	DQ15	101	Vcc	06	DQ33	54	DQ47	102	Vcc
07	DQ2	55	Vss	103	A6	08	DQ34	56	Vss	104	A7
09	DQ3	57	*CB0	105	A8	10	DQ35	58	*CB4	106	BA0
11	Vcc	59	*CB1	107	Vss	12	Vcc	60	*CB5	108	Vss
13	DQ4	61	CLK0	109	A9	14	DQ36	62	CKE0	110	*BA1
15	DQ5	63	Vcc	111	A10	16	DQ37	64	Vcc	112	*A11
17	DQ6	65	/RAS	113	Vcc	18	DQ38	66	/CAS	114	Vcc
19	DQ7	67	/WE	115	DQM2	20	DQ39	68	*CKE1	116	DQM6
21	Vss	69	/CS0	117	DQM3	22	Vss	70	*A12	118	DQM7
23	DQM0	71	*/CS1	119	Vss	24	DQM4	72	*A13	120	Vss
25	DQM1	73	NC	121	DQ24	26	DQM5	74	*CLK1	122	DQ56
27	Vcc	75	Vss	123	DQ25	28	Vcc	76	Vss	124	DQ57
29	A0	77	*CB2	125	DQ26	30	A3	78	*CB6	126	DQ58
31	A1	79	*CB3	127	DQ27	32	A4	80	*CB7	128	DQ59
33	A2	81	Vcc	129	Vcc	34	A5	82	Vcc	130	Vcc
35	Vss	83	DQ16	131	DQ28	36	Vss	84	DQ48	132	DQ60
37	DQ8	85	DQ17	133	DQ29	38	DQ40	86	DQ49	134	DQ61
39	DQ9	87	DQ18	135	DQ30	40	DQ41	88	DQ50	136	DQ62
41	DQ10	89	DQ19	137	DQ31	42	DQ42	90	DQ51	138	DQ63
43	DQ11	91	Vss	139	Vss	44	DQ43	92	Vss	140	Vss
45	Vcc	93	DQ20	141	SDA	46	Vcc	94	DQ52	142	SCL
47	DQ12	95	DQ21	143	Vcc	48	DQ44	96	DQ53	144	Vcc

* Please refer Block Diagram

Block Diagram



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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 to +4.6	V
Voltage on V_{DD} supply to Vss	V_{DD}, V_{DDQ}	-1.0 to +4.6	V
Storage temperature	T_{STG}	-55 to +150	°C
Power dissipation	P_D	16	W
Mean time between failure	MTBF	50	year
Temperature Humidity Burning	THB	85°C/85%, Static Stress	°C-%
Temperature Cycling Test	TC	0°C ~ 125°C Cycling	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Input high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	IOH=-2mA
Output low voltage	V_{OL}	-	-	0.4	V	IOL=2mA
Input leakage current	I_{IL}	-10	-	10	uA	3
output leakage current	I_{oL}	-10	-	10	uA	-

Note: 1. V_{IH} (max) = 2.0V AC .The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC .The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V±0.3V, T_A = 0°C~70°C)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0~A_{12}, BA_0, BA_1)	C_{IN1}	80	100	pF
Input capacitance (/RAS, /CAS, /WE)	C_{IN2}	80	100	pF
Input capacitance (CKE0, CKE1)	C_{IN3}	50	60	pF
Input capacitance (CLK0, CLK1)	C_{IN4}	40	45	pF
Input capacitance (/CS0, /CS1)	C_{IN5}	25	35	pF
Input capacitance (DQM0~DQM7)	C_{IN6}	15	20	pF
Data input/output capacitance (DQ0~DQ63)	C_{OUT1}	10	15	pF

DC CHARACTERISTICS

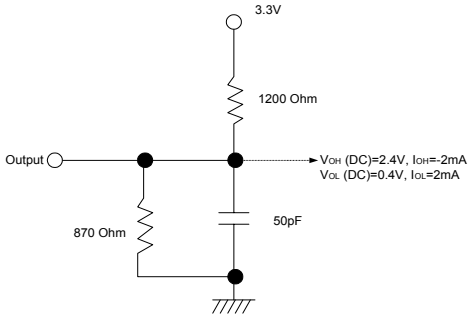
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Value (Typ)	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL}=0mA	1,200	mA	1
Precharge Standby Current in power-down mode	I_{CC2}**P**	CKE≤V_{IL}(max), t_{CC}=10ns	32	mA	
	I_{CC2}**PS**	CKE & CLK≤V_{IL}(max), t_{CC}=∞	32		
Precharge Standby Current in non power-down mode	I_{CC2}**N**	CKE≥V_{IH}(min), /CS≥V_{IH}(min), t_{CC}=10ns Input signals are changed one time during 20ns	256	mA	
	I_{CC2}**NS**	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC}=∞ Input signals are stable	224		
Active Standby Current in power-down mode	I_{CC3}**P**	CKE≤V_{IL}(max), t_{CC}=10ns	96	mA	
	I_{CC3}**PS**	CKE & CLK≤V_{IL}(max), t_{CC}=∞	96		
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3}**N**	CKE≥V_{IH}(min), /CS≥V_{IH}(min), t_{CC}=10ns Input singals are changed one time during 20ns	480	mA	
	I_{CC3}**NS**	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC}=∞ Input signals are stable	400		
Operating Current (Bust Mode)	I_{CC4}	I_{OL}= 0 mA Page Burst 4Banks activated t_{CCD} = 2CLKs	1,360	mA	1
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	1,920	mA	1
Self Refresh Current	I_{CC6}	CKE≤0.2V	80	mA	

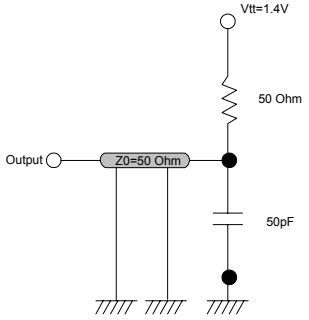
Note: Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 65°C)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf=1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Value	Unit	Note
Row active to row active delay		tRRD(min)	15	Ns	1
/RAS to /CAS delay		tRCD(min)	20	ns	1
Row precharge time		tRP(min)	20	ns	1
Row active time		tRAS(min)	45	ns	1
		tRAS(max)	100	us	
Row cycle time	@Operation	tRC(min)	65	ns	1
Last data in to new col. address delay		tCDL(min)	2	CLK	2
Last data in to Active delay		tDAL(min)	2CLK+20ns	-	
Last data in to row precharge		tRDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data			2	ea	4

Note:
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC Characteristics (T_A = 0 to 65°C, V_{DD} = 3.3V ± 0.3V, Vss= 0V)

Parameter	Symbol	Value	Unit	Note
System clock cycle time	t_{CK}	7.5	ns	1
CK high pulse width	t_{CKH}	2.5	ns	1
CK low pulse width	t_{CKL}(min)	2.5	ns	1
Access time from CK	t_{AC}	5.4	ns	1,2
Data-out hold time	t_{OH}	3.0	ns	1,2
CK to Data-out low impedance	t_{LZ}	0.0	ns	1,2
CK to Data-out high impedance	t_{HZ}	3.0	ns	1
Input setup time	t_{AS}, t_{CS}, t_{DS}, t_{CES}	1.5	ns	1
CKE setup time for power down exit	t_{CESP}	2.0	ns	1
Input hold time	t_{AH}, t_{CH}, t_{DH}, t_{CEH}	0.8	ns	1
Ref/Active to Ref/Active command period	t_{RC}	70.0	ns	1
Active to precharge command period	t_{RAS} (min)	45.0	ns	1
Active command to column command (same bank)	t_{RCD}	20.0	ns	1
Precharge to active command period	t_{RP}	20.0	ns	1
Write recovery or data-in to precharge lead time	t_{DPL}	15.0	ns	1
Active (a) to Active (b) command period	t_{RRD}	15.0	ns	1
Transition time (rise and fall)	t_T (min)	1.0	ns	
Refresh period	t_{REF} (max)	64.0	ms	

Note:
1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.5V.
2. Access time is measured at 1.5V. Load condition is C_L = 50 pF

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	DQM	$BA_{0,1}$	A_{10}/AP	A_{11},A_{12} A_0~A_9	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down	Entry		H	L	H	X	X	X	X	X			
					L	V	V	V					
	Exit		L	H	X	X	X	X	X				
Precharge Power Down Mode	Entry		H	L	H	X	X	X	X	X			
					L	H	H	H					
	Exit		L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note:
1. OP Code: Operand Code
   A_0~A_{12}, BA_0~BA_1: Program keys. (@MRS)
2. MRS can be issued only at both banks precharge state.
   A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
   The automatic precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at both banks precharge state.
4. BA_0~BA_1: Bank select address.
   If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
   If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
   If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
   If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
   If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and both banks are selected.
5. During burst read or write with auto precharge, new read/write command cannot be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at tRP after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edged of a CLK masks the data-in at the very CLK (Write DQM latency is 0),
   but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

Serial Presence Detect Specification

Serial Presence Detect			
Byte No.	Function Described	Standard Specification	Vendor Part
0	Number of Bytes Written into Serial Memory	128bytes	80
1	Total Number of Bytes of S.P.D Memory	256bytes	08
2	Fundamental Memory Type	SDRAM	04
3	Number of Row Addresses on this Assembly	13	0D
4	Number of Column Addresses on this Assembly	10	0A
5	Number of Module Banks on this Assembly	2 bank	02
6	Data Width of this Assembly	64bits	40
7	Data Width Continuation	-	00
8	Voltage Interface Standard of this Assembly	LVTTL3.3V	01
9	SDRAM Cycle Time (highest CAS latency)	7.5ns	75
10	SDRAM Access from Clock (highest CL)	5.4ns	54
11	DIMM configuration type (non-parity, ECC)	Non parity	00
12	Refresh Rate Type	7.8us/Self Refresh	82
13	Primary SDRAM Width	X8	08
14	Error Checking SDRAM Width	None	00
15	Min Clock Delay Back to Back Random Address	1 clock	01
16	Burst Lengths Supported	1,2,4,8,full	8F
17	Number of banks on each SDRAM device	4 bank	04
18	CAS Latency	2 & 3	06
19	CS Latency	0 clock	01
20	Write Latency	0 clock	01
21	SDRAM Module Attributes	Non Buffer	00
22	SDRAM Device Attributes : General	Prec All, Auto Prec, R/W Burst	0E
23	SDRAM Cycle Time (2nd highest CL)	10ns	A0
24	SDRAM Access from Clock (2nd highest CL)	6ns	60
25	SDRAM Cycle Time (3rd highest CL)	-	00
26	SDRAM Access from Clock (3rd highest CL)	-	00
27	Minimum Row Precharge Time	20ns	14
28	Minimum Row Active to Row Activate	15ns	0F
29	Minimum RAS to CAS Delay	20ns	14
30	Minimum RAS Pulse Width	45ns	2D
31	Density of Each Bank on Module	1row of 256MB	40
32	Command/Address Setup Time	1.5ns	15
33	Command/Address Hold Time	0.8ns	08

34	Data Signal Setup Time	1.5ns	15
35	Data Signal Hold Time	0.8ns	08
36-61	Superset Information	-	00
62	SPD Data Revision Code	JEDCE2	02
63	Checksum for Bytes 0-62	-	C3
64-71	Manufacturers JEDEC ID Code per JEP-108E	Transcend	7F,4F
72	Manufacturing Location	T	54
73-90	Manufacturers Part Number	TS64MSS64V 6F	54 53 36 34 4D 53 53 36 34 56 36 46 20 20 20 20 20 20
91-92	Revision Code	-	
93-94	Manufacturing Date	By Manufacturer	Variable
95-98	Assembly Serial Number	By Manufacturer	Variable
99-125	Manufacturer Specific Data	-	0
126	Intel Specification Frequency	-	64
127	Intel Specification CAS# Latency/Clock Signal Support	CL=2, 3 Clock 0,1	F6
128~	Unused Storage Locations	Open	FF